CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A system of securely using decryption keys during Programmable Logic Device (PLD) configuration, comprises:

a microcontroller within the PLD for receiving an encrypted bitstream;

a key storage register coupled to the microcontroller for storing key data;

a decryptor coupled to the key storage register, wherein only the decryptor can read from the key storage register; and

a configuration data register in the PLD, wherein the configuration data register cannot be read by the microcontroller after the decryptor is used.

2. (Original) The system of claim 1 wherein the microcontroller stores key data in the key storage register, but the microcontroller cannot read from the key storage register.

3. (Original) The system of claim 2, wherein the decryptor is a hardware decryptor embedded in an integrated circuit along with the PLD.

4. (Original) The system of claim 1, wherein the decryptor is a software decryptor stored in a memory that uses hardware to enable access to the key storage register based on a memory address.

5. (Original) The system of claim 4, wherein the memory is a ROM having a decryption engine.

6. (Original) The system of claim 1, wherein the microcontroller further receives a configuration boot program along with the encrypted bitstream.

7. (Original) The system of claim 1, wherein the microcontroller, the key register, the decryptor, and the configuration data register are all within the PLD.

8. (Original) The system of claim 1, wherein the microcontroller is an emulated microcontroller in the PLD.

9. (Currently Amended) A system of securely using decryption keys during configuration of an integrated circuit having programmable logic, comprising:

a microcontroller within the integrated circuit for receiving an encrypted bitstream;

a key storage register coupled to the microcontroller for storing key data;

a decryption program stored in a memory that uses a predetermined memory address to enable access to the key storage register; and

a configuration data register in the [[FPGA]] integrated circuit, wherein the configuration data register cannot be read by the microcontroller after the decryption ~~programmed~~ program is used.

10. (Original) The system of claim 9, wherein the memory is a ROM containing a decryption engine.

11. (Original) The system of claim 9, wherein the microcontroller further receives a configuration boot program along with the encrypted bitstream.

12. (Currently Amended) A method of securely using decryption keys during field programmable gate array configuration, comprising the steps of:

receiving an encrypted bitstream at a microcontroller within the field programmable gate array;

loading a decryptor with data from a key register;

loading the decryptor with data from the microcontroller; and

loading a configuration data register with a decrypted bitstream from the decryptor, wherein the configuration data register cannot be read by the microcontroller after the decryptor is used.

13. (Original) The method of claim 12, wherein the method further comprises the step of loading the key register with key data from the microcontroller.

14. (Currently Amended) The method of claim 12, wherein the configuration data register ~~microcontroller can only~~ cannot be read by the microcontroller ~~configuration data register after~~ while the decryptor is used.

15. (Original) The method of claim 12, wherein the microcontroller cannot read from the key register.

16. (Original) The method of claim 12, wherein only the decryptor can read from the key storage register.

17. (Original) The method of claim 12, wherein the steps of loading the decryptor with data from key register and loading the decryptor with data from the microcontroller comprises using a predetermined instruction enabling access to the key storage register based on a known address of a memory storing a decryption engine forming the decryptor.

18. (Original) A system of securely using decryption keys during programmable logic device configuration, comprises:

a memory-mapped key register coupled to a microcontroller data bus;

a decryptor engine stored in non-volatile memory and coupled to the microcontroller data bus; and

logic circuitry limiting access to the key register from the microcontroller data bus using specified addresses of the non-volatile memory.

19. (Original) The system of claim 18, wherein the logic circuitry uses specified addresses of the non-volatile memory by limiting access to minimum and maximum ROM memory addresses using a microcontroller program counter.

20. (Currently Amended) A computer program product comprising:

a computer-usable medium comprising a bitstream that configures a programmable logic device, the computer-usable medium ~~bitstream,~~ comprising:

a configuration boot program portion of the bitstream that ~~for running~~ runs a microcontroller on [[a]] the programmable logic device; and

an encrypted bitstream portion of the bitstream containing encrypted configuration data that when decrypted and loaded into [[for]] a configuration data register on the programmable logic device configures the programmable logic device,

wherein the configuration boot program further comprises instructions for a decryptor, wherein the configuration boot program stores the instructions for the decryptor.

21. Cancelled.

22. (Currently Amended) The computer program product [[bitstream]] of claim 20, wherein the [[said]] configuration boot program comprises instructions for a decompressor.